

**Model: uHost-BF1**



- High Performance DSP Blackfin ADSP-BF533 from Analog Devices, Inc.
- Cyclone EP1C3T144I7 FPGA for customer projects
- Microchip PIC18F24 for power good monitoring and HASP customer options
- 70 pin connector for FPGA interface
- 3 connectors for Blackfin on-chip interfaces
- Industrial temperature range (-40 °C...+85 °C)

The module allows updating user software, FPGA projects and other sectors of Flash-ROM in them without opening the device cover via RS-422 serial port with the help of the corresponding service PC software.

The diagram illustrates the system architecture, centered around the **ADSP-BF533** (DD1) and the **FPGA Cyclone** (DD6). The ADSP-BF533 is connected to various external components and internal memory blocks:

- External Interfaces:**
  - X5 JTAG** (Blue box) and **DD3 TTL / RS422** (Yellow box) are connected to the top of the ADSP-BF533.
  - DD5 29.491 MHz** (Green box) and **RTC 32768 Hz** (Green box) provide clock signals to the ADSP-BF533.
  - X1 Reset** (Blue box) is connected to **DD4** (Yellow box), which then connects to the ADSP-BF533.
  - X3 PICProg** (Blue box) is connected to **DD13  $\mu$ C** (Orange box), which in turn connects to the ADSP-BF533.
  - X10 JTAG** (Blue box) is connected to the bottom of the ADSP-BF533.
- Internal Memory and Logic:**
  - DD7 FLASH** (Orange box) is connected to the ADSP-BF533 and **DD2 SDRAM** (Orange box).
  - DD2 SDRAM** is connected to the ADSP-BF533 and **DD8 CPLD MAX** (Orange box).
  - DD8 CPLD MAX** is connected to the ADSP-BF533 and **DD6 FPGA Cyclone** (Orange box).
  - DD6 FPGA Cyclone** is connected to the ADSP-BF533 and has an **in/out** interface (Grey box) to the right.
- Other Components:**
  - LD\_1** and **LD\_2** (Light blue boxes) are connected to **DD13  $\mu$ C**.
  - LD\_3** and **LD\_4** (Light blue boxes) are connected to **DD8 CPLD MAX**.

The ADSP-BF533 and FPGA Cyclone are connected via a bidirectional interface labeled **SPI, DPI, SPORT** (Grey box).

## Specification

System	
CPU	DSP Analog Devices Blackfin ADSP-BF533 @ 470 MHz
RAM	32 Mbytes SDRAM @ 117 MHz
Flash ROM	4 Mbytes
FPGA	Altera FPGA Cyclone EP1C3T144I7 from Intel Corp.
JTAG	Analog Devices JTAG connector (not soldered), Altera FPGA JTAG connector for debugging, diagnostics and manufacturing
RTC	With connector for external battery, 4 pin connector
Microchip PIC	PIC18F24 for power good monitoring and HASP options
Interfaces	
Blackfin on-chip UART, RS-422	For servicing (user software, FPGA project update) and debugging
SPI	1 interface with 4 chip selects, can be program as GPIO pins, 10 pin connector
PPI	1 interface with 8 bit data bus, can be program as GPIO pins, 14 pin connector
SPORT	Dual-channel synchronous serial port, 1 interface, 10 pin connector
Expansion connector	For optional interfaces to FPGA, 53 GPIO in 70 pin connector
LEDs	2 user LEDs
Power, environmental and mechanical	
Power Supply	+5 V, 120... 330 mA (depends on SDRAM and FPGA usage)
Temp. range	-40 °C...+85 °C
Dimensions	80 mm x 48 mm x 8 mm

## Versions of delivery

### 1. uClinux OS:

- u-boot boot loader;
- uClinux drivers support for module devices;
- demonstration FPGA project written into Flash ROM (with source code).

### 2. Non-OS:

- boot loader written into Flash ROM;
- demonstration FPGA project written into Flash ROM (with source code);
- PC software under Microsoft Windows for flashing user software and FPGA project via serial RS-422 interface;
- Blackfin software examples with source code.



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